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Review On Hybrid Modular Multilevel Converter H-bridge Cells for HVDC Applications

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ABSTRACT- H-bridge-based multilevel converters (e.g., cascaded H-bridge converters) benefit from modularity and scalability. However, they suffer from the complexity and costs associated with a large count of semiconductor switches, together with their drivers and peripheral circuits, as well as higher conduction losses as compared to half-bridge-based counterparts, as two switches in each sub module must simultaneously conduct to provide a current path. To reduce the number of active switch semiconductors and conduction losses, this paper proposes novel multilevel converters with symmetrical half-bridge sub modules. The symmetrical half-bridge sub module features a bipolar voltage output, a reduced switch count, and simplicity. Further, this paper proposes a sensor less voltage balance scheme that successfully gets rid of capacitor voltage mismatch problems through diodes and sub module parallelization. This scheme can greatly reduce capacitor voltage ripples, thereby allowing the saving of dc capacitances, particularly in the case of numerous sub modules. Finally, simulation and experimental results validate the superiority of the proposed multilevel converters and voltage balance scheme. In the first control layer, the voltage vector of cells is adjusted so that the active power is uniformly distributed among the cells. In the second control layer, the switching redundancies of FNPC are used to provide voltage balancing. The introduced balancing scheme not only provides voltage balance among capacitors, but also distributes the reactive power equally among the cells and increases the reliability in this way. The performance of the proposed control is validated through simulation in MATLAB/SIMULINK environment and experimental results based on a single-phase nine-level HC-FNPC-based STATCOM laboratory prototype

Keywords – Cascaded H-bridge (CHB), half-bridge, modular multilevel converter (MMC), multilevel converter, sensor less voltage balance. DC fault reverse blocking capability.

I. INTRODUCTION

The development of multilevel converters promises to advance high-voltage dc (HVdc) and ac (HVac) transmissions medium voltage motor drive (e.g., automotive propulsion and marine drive) renewable generation power quality enhancement medical applications such as pulse synthesizers for noninvasive magnetic brain stimulation energy storage integration, and electric vehicles Attractive features of multilevel converters include the use of low-voltage semiconductors for high-voltage treatments, high power quality, the possibility of removing passive filters low electromagnetic interference noises (due to reduced voltage and current changing rates), high reliability and redundancy, and diminished common mode problems Despite these identified advantages, multilevel converters are burdened by the complexity and costs associated with large amounts of active and passive components. Such shortcomings push forward the research of simpler multilevel converters

Recently, maintaining the power quality within standard limits draws attention to avoid power quality issue Due to the undesirable performance of conventional compensators (such as static VAR compensator (SVC) that depends on the grid parameters to a great extent and also have a low dynamic response) and the rapid development of power electronic devices, the flexible alternating current transmission system (FACTS) devices are employed to mitigate power quality (PQ) problems. Among them, Statics synchronous Compensator (STATCOM), which is connected in shunt to the transmission and distribution networks leads to optimum use of the power transfer capability by exchanging the reactive power. It also improves the PQ by flicker suppression caused by non-linear loads, voltage stabilization during transients, improving the power factor, oscillation damping, and reducing ohmic loss in lines

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II. SVPWM

Space Vector Pulse width Modulation (SVPWM) produces the suitable gate drive waveform for each PWM cycle. The inverter is dealt with as one single unit and can join diverse switching states (number of switching states relies upon levels). The SVPWM gives one of a kind switching time estimations to each of these states. This method can without much of a stretch be changed to larger amounts and works with a wide range of multilevel inverters (cascaded, capacitor braced, diode cinched). The three vectors that shape one triangle will give obligation process duration to each, giving the coveted voltage vector.

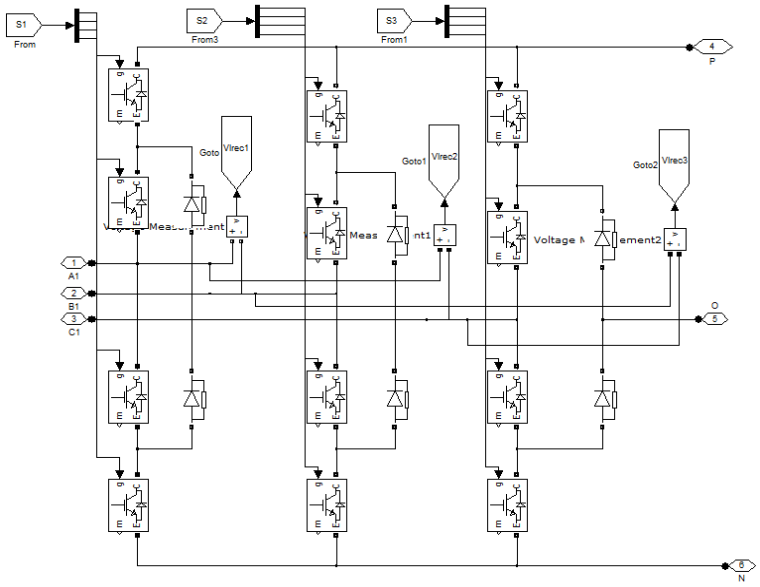

Figure: Proposed Indirect Matrix Converter Circuit

III. FAULT-TOLERANCE

Fault tolerance system includes no of following advances, each progression is related with particular capacity consequently they can be connected independently during the time spent fault taking care of and the life cycle of fault taking care of is delineated in Fault Detection: One of the most essential parts of fault taking care of in RTDS is distinguishing a fault immediately and disengaging it to the proper unit as quickly as would be prudent. In disseminated system there are no main issues for post from which the whole system can be seen immediately consequently fault identification remains a key issue in appropriated system. Uncovers the effect of speedier fault finders in Real Time System. Outline objectives and engineering for fault location in grid has been talked about further. Commonly utilized fault recognition procedures are Consensus, Deviation Alarm and Testing.

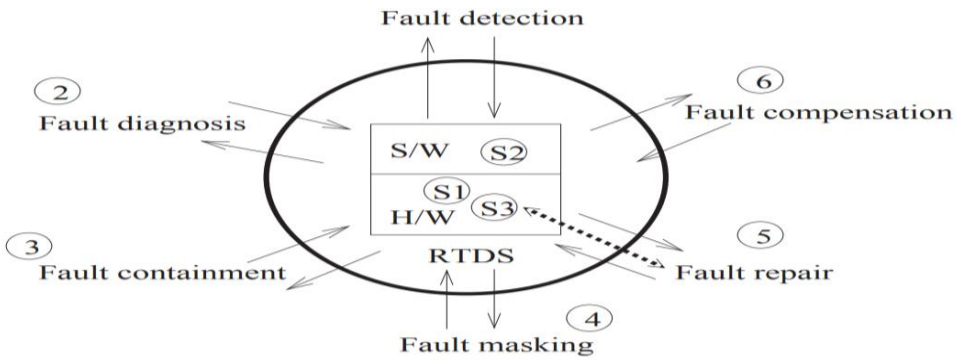

Figure: Life Cycle of Fault Handling

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IV. MMC SYSTEM

In the initial segment of this examination a macro model is accommodated the MMC structure. The implied found the center estimation of model energizes considerations and examinations without thinking about the impacts of the music at the trading repeat, influencing the investigation to quick and direct. Measuring parameters are accommodated the reactive components (branch inductors and cell capacitors) for two distinctive approaches. A first approach assumes a present control, which acts specifically on the AC output current (one current control for each stage). Under this condition, another setup is similarly proposed for the branch inductor with a particular true objective to improve the framework exhibitions. The second approach proposes two current circles for each stage, each of which acts on the current of each inductor. For the two techniques, recreations are performed to favor the examination.

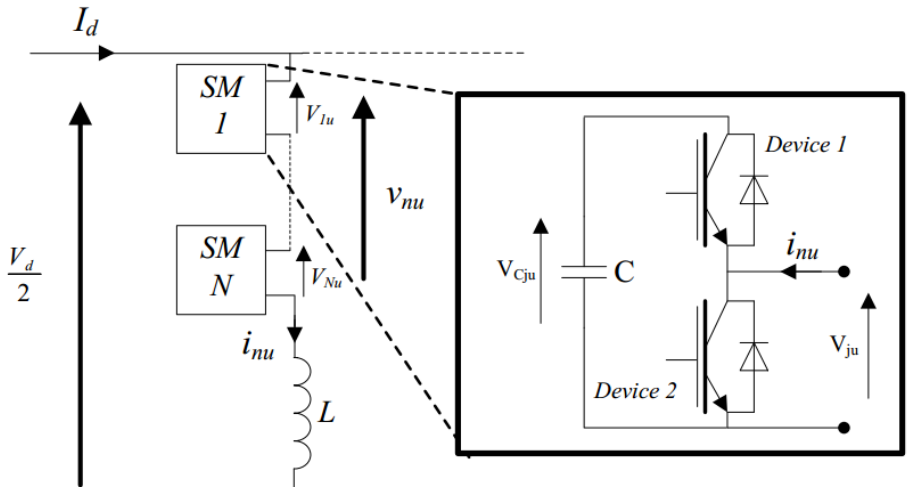

Figure: MMC structure is composed by single cells.

V. ADDITIVE AND MULTIPLE FAULTS

In the above exchanges, shortcomings/disappointments are grouped and displayed, as indicated by their physical areas, into framework flaws, actuator blame and sensor issues. It should be brought up that these issues can likewise be displayed by their consequences for the framework yields and the framework elements. For this situation, they are grouped into added substance and multiplicative deficiencies. So as to be predictable with the demonstrating of the shortcomings portrayed in the past areas, in this segment, the added substance and multiplicative issues are likewise displayed in two diverse frameworks.

VI. STRUCTURE OF MATRIX CONVERTER

The switch duty-cycle and switching-sequences are determined according to control-command-signals. The control-command-signals specify the desired input-currents/output-voltages of the MC at input/output fundamental frequency of the MC. Assuming the switching-frequency are much higher than the input/output fundamental frequency then switching-sequences can be arbitrarily selected and the switch duty-cycles are determined according to control-command signals. Basically, a matrix converter (MC) is formed by 9 bidirectional switches, as appeared in where each dot of the grid allude to an association between the yield and the input terminals. The converter is normally fed at the input side by a three phase voltage source and it is associated with an inductive load at the yield side.

VII. CONCLUSION

This paper presented the basic operational principle, modulation and capacitor voltage balancing of an emerging hybrid cascaded multilevel converter with dc side cascaded H-bridge cells. Simulations and experimentation were used to confirm the practicality of the hybrid cascaded converter, including its scalability to high-voltage applications. It has been shown that the hybrid cascaded converter with dc side cascaded H-bridge cells can operate over the entire P-Q envelope normally required for HVDC

converters, without capacitor voltage balancing problems, and with voltage stresses on the converter switches evenly distributed. The comparison has been carried out assuming either the same cycle period or the same switching frequency. The obtained results clearly emphasize the effectiveness of the proposed approach through THD analysis. The total harmonic distortion SVPWM based multi level indirect matrix converter for nonlinear loads is 1.90 %, 1.11% and 1.17%. Here, is it clearly visible that % THD is less in case of SVPWM as compare existing approach. Hence, it can be easily conclude that the proposed Technique is more efficient in eliminating harmonics.

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